MMS – MCD
Application Team

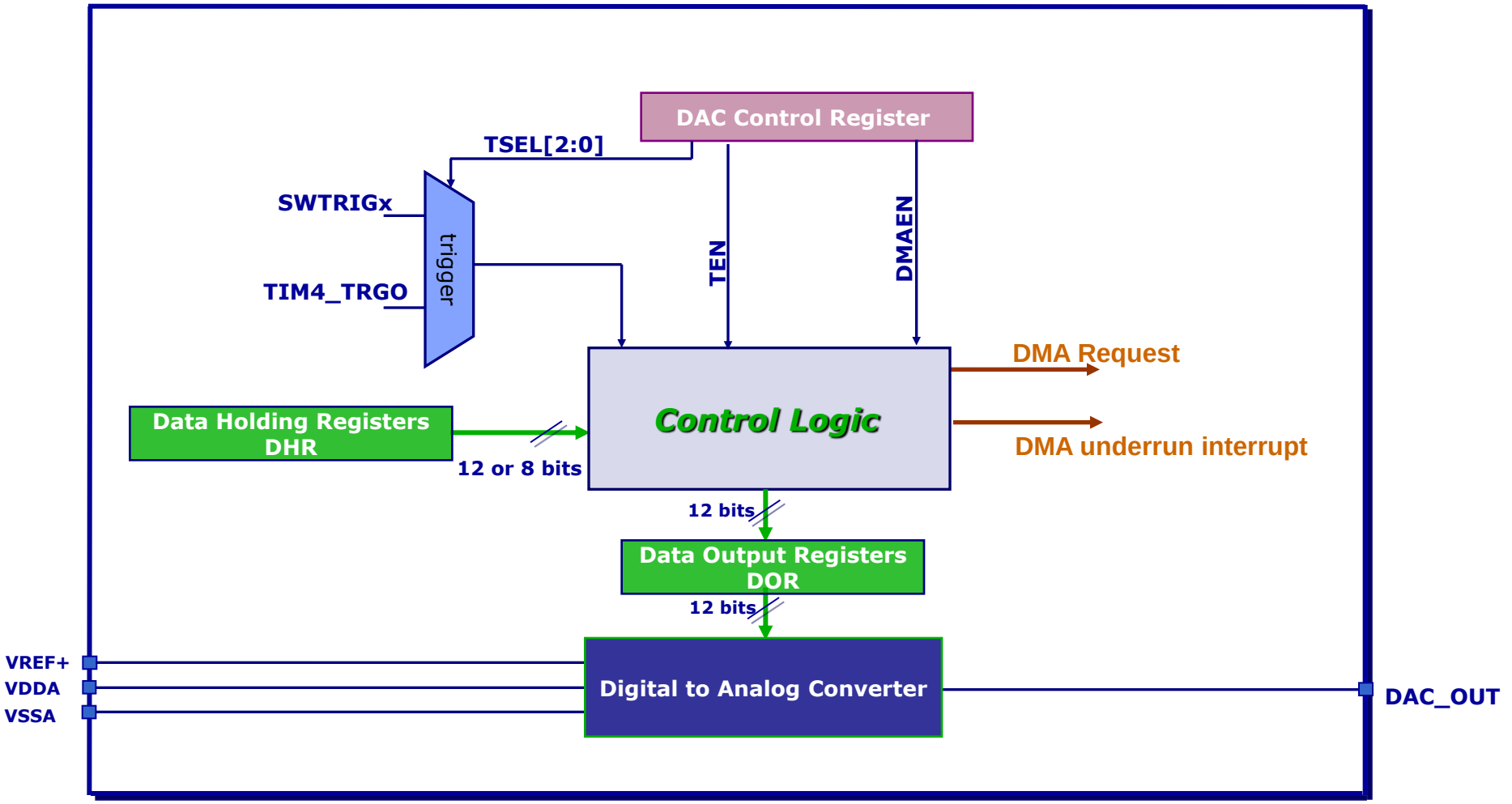
STM8L Training Slides

Digital-to-Analog Converter (DAC)

DAC Features

- 8-bit or 12-bit DAC, 1µs settling time converter (code to code)
- Internal buffer can drive load up to 5 kΩ / 50 pF
- DAC supply requirement: 1.8V to 3.6 V
- DAC outputs range: $0 \leq V_{OUT} \leq VREF+$
  - Note : ADC and DAC share the same VREF+ / VDDA / VSSA
- Left or right data alignment in 12-bit mode
- Synchronized update capability using TIM4
- DMA capability
- External triggers for conversion (timer)

DAC Block Diagram



DAC Output Voltage

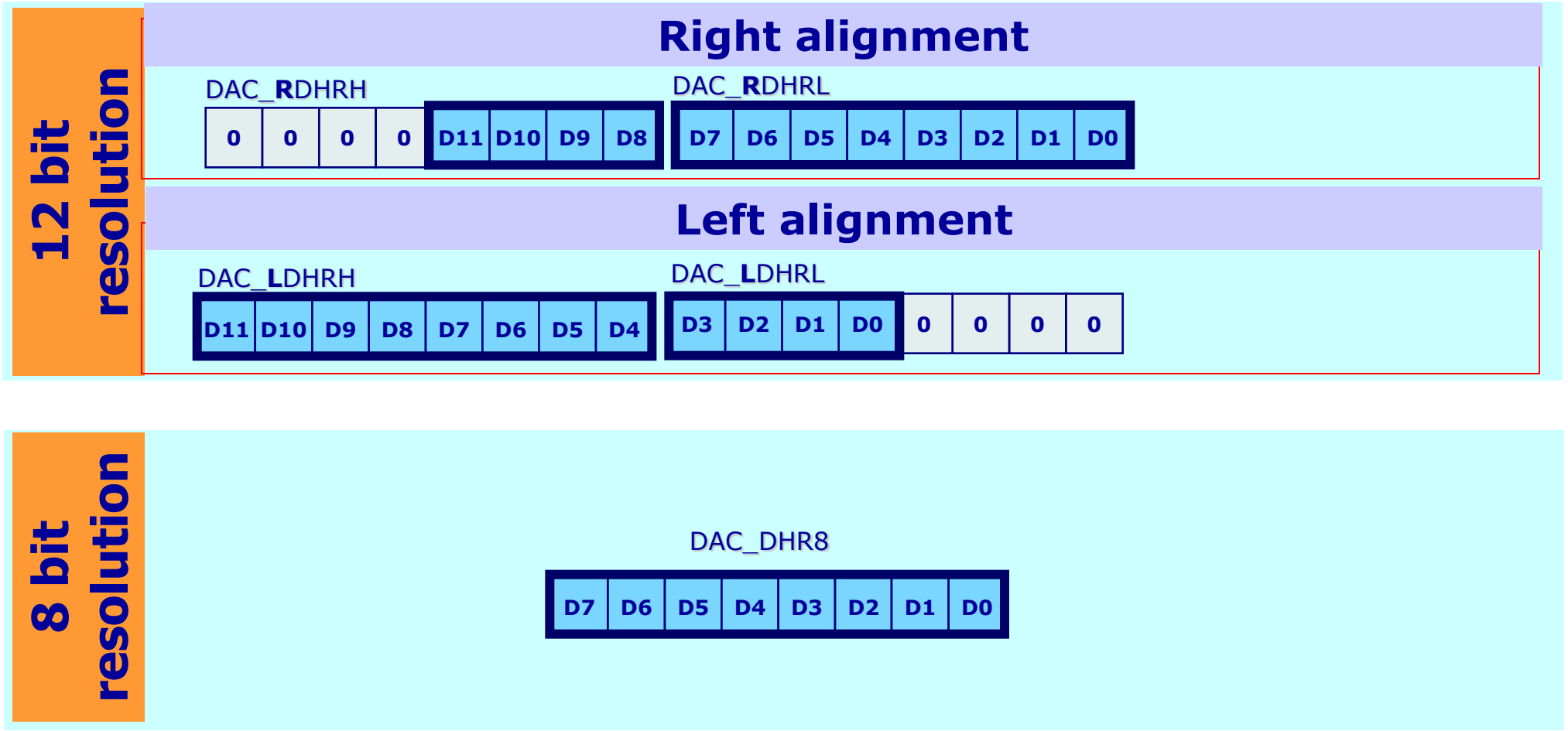
- The analog output voltage on the DAC channel pin is determined, for both 8bit and 12bit resolution modes, as:

$$\textbf{DAC Output voltage} = V_{REF+} \times (DOR / 4095)$$

- Integrated output buffer:
  - can be enabled/disabled by BOFF bit
  - used to reduce the output impedance

DAC Data Resolution / alignment

Separate data holding registers (DHR) for each data alignment and resolution



DAC Conversion triggers

- Programmable DAC conversion triggers
- DAC Conversion is started :
  - **Automatically** (without triggers) – after writing to data holding registers (DHR)
  - by **using triggers**

- 2 possible conversion Triggers :
  - **Software trigger :** by setting the SWTRIG bit
  - **Hardware trigger :** Timer4 TRGO input

DMA Capabilities

- DAC is connected to DMA1 channel 3.

- DAC DMA request is generated when an external trigger occurs. The request indicates that the value of the data holding registers (DHR) is then transferred to the Data output registers (DOR)

- DAC DMA underrun interrupt is generated when the next trigger event occurs while the previous DMA request is still pending. This may happen, for instance, when the DAC trigger frequency is higher than the DMA request servicing process

Quiz

- How many DAC channels are in the STM8L15x microcontroller ?

  _____

- What are the possibilities to start a DAC channel conversion?

  _____

- Which is the DMA channel connected to the DAC?

  _____

- When a DAC DMA underrun interrupt may be happen.

  _____

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